REMARKS

Interview Summary

Applicant's representative wishes to thank Examiner Farahani for the courtesies extended during the interview of January 12, 2007. During the interview, the merits of the rejections were discussed. While no agreements were reached, Examiner Farahani indicated that amending the claims to specify that the "depositing" step occurs subsequent to the "forming a gate" step; and further amending the claims to recite "selectively depositing," might help to overcome the rejections of record.

Accordingly, claims 1 and 12 have been amended to recite "after forming the gate, selectively depositing," as shown in the above Amendments to the Claims section. All other amendments to the claims were not made for reasons of patentability, but instead were made to correct grammatical errors and/or typographical errors in the claims, and are not intended to narrow the scope of the claims.

Rejections under 35 USC §102

The Office has rejected claims 1, 2, 8, 12, 24 and 25 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,734,108 ("Jin"), for the reasons set forth at page 2 of the outstanding office action. Applicant respectfully traverses the rejection.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. See MPEP 2131.

Independent claims 1 and 12 are both directed to a method of fabricating a semiconductor device including, *inter alia*, forming a gate (or "doped gate," in the case

of claim 12), and "after forming the gate, selectively depositing an oxide material comprising at least one material from the group consisting of AlO_3, ZrO_2, $HfO_2(AlHf)O_x$, HfO_2, La_2O_3, Y_2O_3, silicon oxynitride, and hafnium silicon oxynitride substantially on the top surface of the gate, as well as over the semiconductor substrate, the opposing side surfaces of the gate being substantially free of the oxide material."

Jin does not teach selectively depositing an oxide material on a gate, as recited by the claims. Instead, Jin teaches non-selectively depositing a gate top insulating layer 610 over a gate conducting layer 608 prior to forming a gate, as shown in FIG. 6A, and then etching both layers 610 and 608 to form a gate structure, as shown in FIG. 6B. *See also,* Jin, Column 9, lines 60-63 and column 10, lines 20-22. A sidewall layer 616 is then formed, also by a non-selective technique, as illustrated in FIG. 6C, followed by etching to form sidewalls 618-1 and 618-2. Column 10, lines 23-29 and 59-65. Because Jin fails to teach selectively depositing an oxide material on a gate, every limitation of the claims is not taught.

Claims 2, 8, 24 and 25 depend either directly or indirectly from, and therefore contain all the limitations of, claims 1 and 12. Therefore, for at least the reasons set forth above, Jin also fails to teach every limitation of these claims.

Because Jin fails to teach every limitation of the claims, no *prima facie* case of anticipation exists. Accordingly, applicant requests that the rejection be withdrawn.

Rejections under 35 USC §103

The Office has rejected claims 9, 10, and 18 as being unpatentable under 35 USC §103 over Jin in view of U.S. Patent No. 5,814,543 ("Nishimoto"), for the reasons set forth at page 3 of the Office Action. Claim 13 stands rejected as being unpatentable

under 35 USC §103 over Jin alone, for the reasons set forth at page 3 to 4 of the Office Action. Claims 11 and 19 stand rejected as being unpatentable under 35 USC §103 over Jin, and Jin in view of Nishimoto, for the reasons set forth at page 4 of the Office Action. Finally, the Office has rejected claims 4, 6, 14, and 15 as being unpatentable under 35 USC §103 over Jin in view of U.S. Patent No. 6,303,490 ("Jeng"), for the reasons set forth at page 4 of the Office Action. Applicants respectfully traverse these rejections.

None of the above references, including Jin, Nishimoto and Jeng, either taken separately or in combination, teach or suggest applicants claimed invention. Nishimoto and Jeng fail to cure the deficiencies of the Jin reference, because neither Nishimoto nor Jeng teach or suggest forming a gate and, after forming the gate, selectively depositing an oxide material, as set forth in the instant claims. Instead, Nishimoto teaches depositing an oxidation resistant mask 5 on a polycrystalline film, and then etching to form a gate material 8. See Nishimoto, FIG. 6 and column 11, lines 24-33. Jeng teaches an anisotropic deposition process employed in a dual damascene process to form an interconnect, and does not appear to be related to forming a gate structure. See Jeng, column 3, lines 10-28; column 4, lines 18-27; and FIG. 2.

Because none of the applied references supply the missing teachings of Jin, no *prima facie* case of obviousness has been made. For at least this reason, applicant requests that the rejection be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully requests reconsideration of this application and the timely allowance of the pending claims.

In the event that the Examiner determines that any outstanding issues remain that would prevent an immediate allowance of this application, it is requested that the Examiner contact applicants' undersigned representative, Matthew Whipple, at (703) 917-0000, Ext. 103, in order that the issues be quickly resolved and the case moved to allowance.

Please grant any extensions of time required to enter this response and charge any additional required fees to Texas Instruments' Deposit Account 20-0668.

Respectfully submitted,

Dated: January 25, 2007

By: Barbara A. Fisher (Reg. No. 31,906)
for Matthew L. Whipple
Reg. No. 47,217

Timothy M. Hsieh
Reg. No. 42,672

MH2 TECHNOLOGY LAW GROUP
703.917.0000